WHAT IS CLAIMED IS:

1. A measuring device for measuring the coupling capacitance between two lines of an integrated circuit structure, the measuring device being used to measure a first coupling capacitance C and a second coupling capacitance C_{dummy} of a target line of an integrated circuit structure of length **L**, the substrate of the integrated circuit structure being grounded, the measuring device comprising:

a first measuring set, comprising:

a first branch circuit, comprising:

a first transistor and a second transistor connected in series at a first node, wherein a terminal of the first transistor is connected to a high voltage and a terminal of the second transistor is connected to a low voltage, the first transistor is electrically opposite to the second transistor;

a second branch circuit, comprising:

a third transistor and a fourth transistor connected in series at a second node, wherein a terminal of the third transistor is connected to the high voltage and a terminal of the fourth transistor is connected to the low voltage, the third transistor is electrically opposite to the fourth transistor,

wherein the first transistor is the same as the third transistor, the second transistor is the same as the fourth transistor, the control terminals of the first transistor and the third transistor are connected and driven by a first

voltage signal, and the control terminals of the second transistor and the fourth transistor are connected and driven by a second voltage signal, the first voltage signal and the second voltage signal don't simultaneously turn on the transistors of each branch circuit;

a first test structure, coupled to said first node, comprising:

a first line connected to said first node, the first line being the same as the target line and longer than the target line; and

two second lines placed at the two sides of said first line, which are parallel to and equally away from said first line and are grounded,

wherein the distance and parallel overlap length between said first line and each of said two second lines are S and X+L, respectively; and

a second test structure, coupled to said second node, comprising:

a third line connected to said second node, said third line being the same as said first line and shorter than said first line; and

two fourth lines placed at the two sides of said third line, which are parallel to and equally away from said third line and are grounded,

wherein the distance and parallel overlap length between said third line and each of said two fourth lines are S and X respectively, said two fourth lines are the same as said two second lines and shorter than said two second lines,

wherein the length of said first line minus the length of said third line equals L, the total loading capacitance of said first node derived from

said first test structure with respect to ground minus that of said second node derived from said second test structure with respect to ground is said first coupling capacitance C of said target line of length **L**; and

a second measuring set, comprising:

a third branch circuit, comprising:

a fifth transistor and a sixth transistor connected in series at a third node, wherein a terminal of the fifth transistor is connected to said high voltage and a terminal of the sixth transistor is connected to said low voltage, the fifth transistor is electrically opposite to the sixth transistor;

a fourth branch circuit, comprising:

a seventh transistor and an eighth transistor connected in series at a fourth node, wherein a terminal of the seventh transistor is connected to the high voltage and a terminal of the eighth transistor is connected to the low voltage, said seventh transistor is electrically opposite to said eighth transistor,

wherein the fifth transistor and the seventh transistor are the same as the first transistor, the sixth transistor and the eighth transistor are the same as the second transistor, the control terminals of the fifth transistor and the seventh transistor are connected and driven by said first voltage signal, and the control terminals of the sixth transistor and the eighth transistor are connected and driven by said second voltage signal, the first voltage signal and the second voltage signal don't simultaneously turn on the transistors of each branch circuit;

a third test structure, coupled to said third node, comprising:

a first subordinate structure comprising:

a fifth line of length y+L, said fifth line being the same as said target line and longer than said target line; and

two sixth lines of length y+L placed at the two sides of said fifth line, which are parallel to and equally away from said fifth line, said two sixth lines being the same as said fifth line,

wherein the distance and parallel overlap length between said fifth line and each of said two sixth lines are s and y+L, respectively; and

a second subordinate structure comprising:

two parallel seventh lines of length y spaced a distance of s apart, wherein the parallel overlap length between the two seventh lines is y, said two seventh lines being the same as said fifth line,

wherein said five lines are shorted together and connected to said third node; and

a fourth test structure, coupled to said fourth node, comprising:

a third subordinate structure comprising:

three parallel eighth lines of length y spaced a distance of s apart, said three eighth lines being the same as said fifth line, wherein the parallel overlap length between the three eighth lines is y; and

a fourth subordinate structure comprising:

two parallel ninth lines of length y+L spaced a distance of s apart, said two ninth lines being the same as said fifth line, wherein the parallel overlap length between the two ninth lines is y+L,

wherein the five lines are shorted together and connected to said fourth node,

wherein the total loading capacitance of said third node derived from said third test structure minus that of said fourth node derived from said fourth test structure is said second coupling capacitance C_{dummy} of said target line of length L.

2. The measuring device of claim 1, wherein said first coupling capacitance C essentially includes a line-to-line capacitance C_c between a part of said first line of length L and each of said two second lines, a fringe capacitance C_f between each lateral edge of said part and the substrate of the integrated circuit structure, and an area capacitance C_a between the bottom area of said part and the substrate; said first coupling capacitance C is equal to $2C_c + 2C_f + C_a$.

3. The measuring device of claim 1, wherein said second coupling capacitance C_{dummy} essentially includes a fringe capacitance C_f between each

lateral edge of a part of said fifth line of length **L** and the substrate of the integrated circuit structure, and an area capacitance C_a between the bottom area of said part and the substrate; said second coupling capacitance C_{dummy} is equal to $2C_f + C_a$.

4. The measuring device of claim 1, wherein all of said lines of said four test structures are in a same metallization layer formed on the substrate of the integrated circuit structure.

5. The measuring device of claim 1, wherein said first transistor, said third transistor, said fifth transistor and said seventh transistor are PMOS field effect transistors.

6. The measuring device of claim 1, wherein said second transistor, said fourth transistor, said sixth transistor and said eighth transistor are NMOS field effect transistors.

7. A method for measuring a line-to-line coupling capacitance C_c between a line A and a line B of an integrated circuit structure of length **L**, the substrate of the integrated circuit structure being grounded, the method comprising:

employing said first measuring set of claim 1, wherein said first line is the same as said line A and said two second lines are the same as said line

B, measuring a first average current I_1 during a first period of time flowing through said first branch circuit and a second average current I_2 during said first period of time flowing through said second branch circuit, and calculating a first capacitance C from the equation $C = (I_1 - I_2)/(V_{dd} * f)$,

wherein V_{dd} is said high voltage of claim 1 and f is the clock frequency of said voltage signals of claim 1;

employing said second measuring set of claim 1, wherein said fifth line, said two sixth lines, said two seventh lines, said three eighth lines and said two ninth lines are the same as said line A, measuring a third average current I_3 during a second period of time flowing through said third branch circuit and a fourth average current I_4 during said second period of time flowing through said fourth branch circuit, and calculating a second capacitance C_{dummy} from the equation $C_{dummy} = (I_3 - I_4)/(V_{dd} * f)$, wherein V_{dd} is said high voltage of claim 1 and f is the clock frequency of said voltage signals of claim 1; and

determining said line-to-line coupling capacitance C_c between said line A and said line B according to the formula $C_c = (C - C_{dummy})/2$.

8. The method of claim 7, wherein said first capacitance C essentially includes said line-to-line coupling capacitance C_c between said line A and said

line B of length L, a fringe capacitance C_f between each lateral edge of said line A and the substrate of the integrated circuit structure, and an area capacitance C_a between the bottom area of said line A and the substrate; said first capacitance C is equal to $2C_c + 2C_f + C_a$.

9. The method of claim 7, wherein said second capacitance C_{dummy} essentially includes said fringe capacitance C_f between each lateral edge of said line A and the substrate of the integrated circuit structure, and said area capacitance C_a between the bottom area of said line A and the substrate; said second capacitance C_{dummy} is equal to $2C_f + C_a$.

10. The method of claim 7, wherein all of the lines of the test structures of said first measuring set and said second measuring set of claim 1 are in a same metallization layer formed on the substrate of the integrated circuit structure.

11. The method of claim 7, wherein the transistors of said first measuring set and said second measuring set of claim 1 connected to said high voltage V_{dd} are PMOS field effect transistors.

12. The method of claim 7, wherein the transistors of said first measuring set and said second measuring set of claim 1 connected to said low voltage of claim 1 are NMOS field effect transistors.

13. The method of claim 7, wherein said line-to-line coupling capacitance C_C between said line A and said line B is less than one femtoFarad.